SIMPLE RISC PROCESSOR MICROARCHITECTURE

v.1.0

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1. Processor pipeline:

The Simple RISC Processor main blocks are sketched in figure 1.

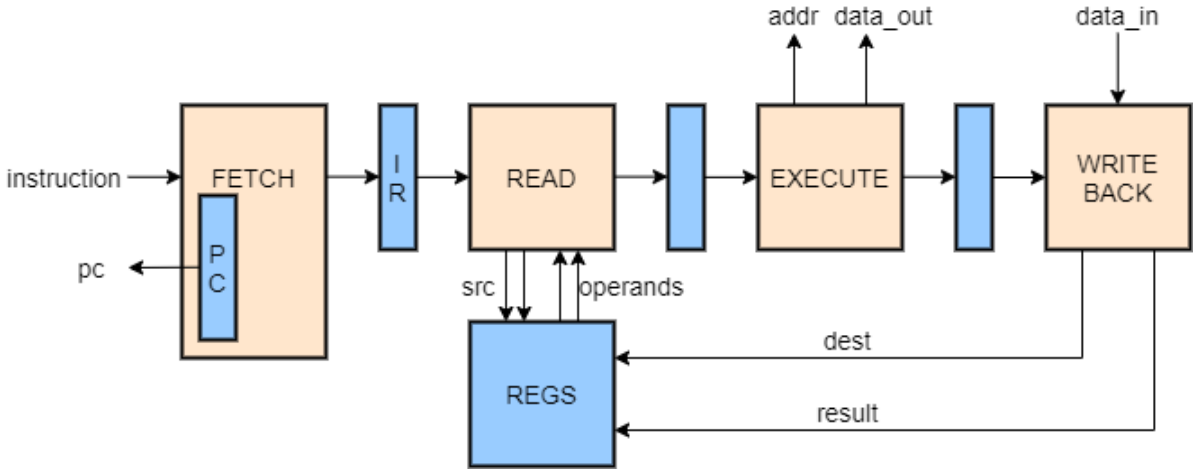

Figure 1
Simple RISC Processor Pipeline.
All registers are shaded blue; the combinational blocks are yellow shaded.

The processor is a 4 stage pipeline:

1. The FETCH stage keeps and updates the program counter (PC), and reads (fetches) instructions from the program memory. The pipeline register at its output, where the fetched instruction is registered, may be assimilated with the instruction register (IR).
2. The READ stage reads the instruction operands from the source registers. For some instructions (LOADC, SHIFTL, SHIFTR, SHIFTRA, JMPR and JMPRcond) one of the operands comes from the instruction itself (constant, offset, value etc.).
3. The EXECUTE stage does the actual computation for the arithmetic and logic instructions and delivers the memory address (addr) for the LOAD and STORE instructions. It sends out the data to be sent to the memory (data_out) for the STORE instruction. For any jump instruction the EXECUTE stage computes the new program address value to be loaded into the PC.
4. The last stage, WRITE BACK, sends the result to the register set, together with its destination. For the LOAD instruction, instead of sending the result coming from the EXECUTE, the WRITE BACK stage sends the data that comes from the memory (data_in). Some instructions (STORE, JMP, JMPR, JMPcond, JMPRcond, NOP and HALT) should not write into the register set.

The reset clears the PC, the registers of the register set and all pipeline registers.