SIMPLE RISC PROCESSOR MINISYSTEM

v.1.0

1 apr 2018

1. Overall minisystem architecture

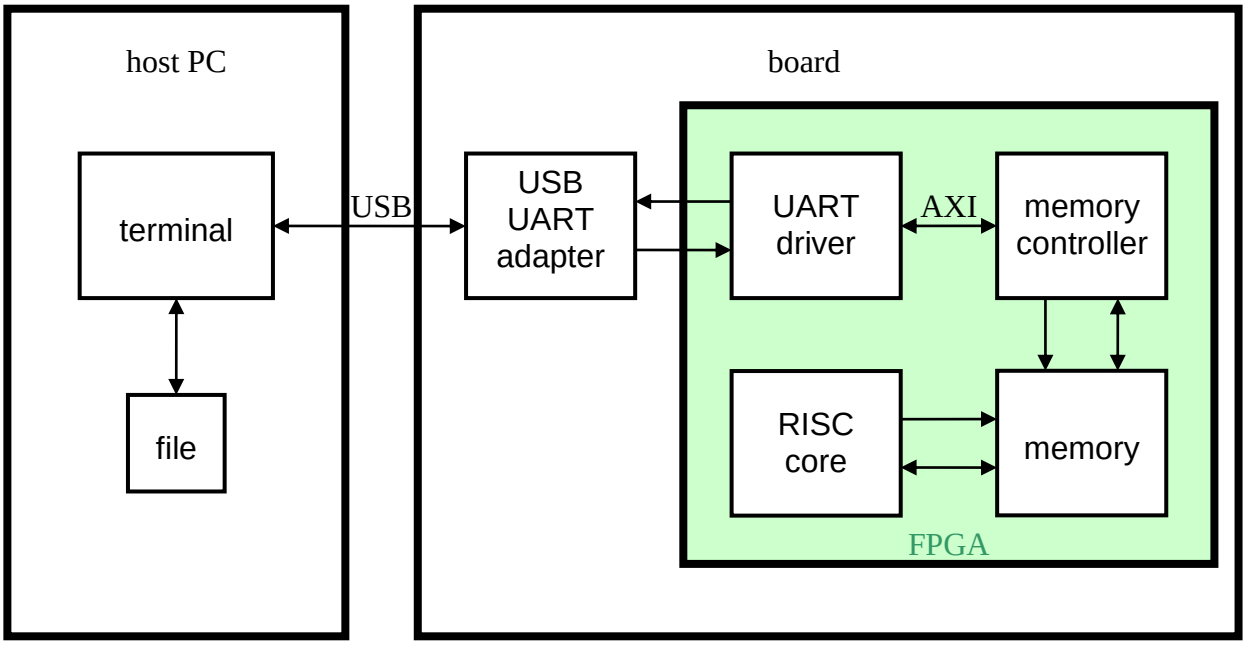

Figure 1
Simple RISC test minisystem

The Simple RISC computer comprises the Simple Risc core, the program memory and the data memory. The program and the data memories are seen by the RISC core as separate memories, with separate access ports for instructions and data, but they may reside in the same physical memory (though using disjoint areas in its memory space).
Either common or separate, the physical memory is built from RAM blocks of appropriate size. The memory has two interfaces, one with the core (with separate instruction and data ports), the other with the memory controller.
The memory controller allows memory initialization or memory update from an outside source and memory content dump to an external destination. For the external access the FPGA system uses a serial interface (UART). The UART-USB physical driver ensures a virtual UART communication between the FPGA system and the host PC.
On the PC side a proper terminal application drives the virtual UART connection (through a physical USB, but the details are left to the OS to manage) and ensures the file upload to, or download from the Simple RISC memory.