Cyber-Physical Society - *iDemocracy*

Gheorghe M. Ştefan

Politehnica University of Bucharest, Romania
(Tel: +40212302714; e-mail: gstefan@arh.pub.ro).

Abstract: The concept of Cyber-Physical Society (CPSo) expands the concept of Cyber-Physical Systems (CPS) by including aspects related to *knowledge*, *culture* and *society*. Embedding computation in the control of our fast evolving society means mainly to trigger self-organizing mechanisms at any level in our complex world. The way democracy is exercised must benefit explicitly from the tremendous development of the information and communication technologies (ICT). ICT has a very big impact on various aspects of our life, but is missing a coherent approach for designing the appropriate environment for the benefit of people in their struggle with a ubiquitous corrupt political class, weak state and voracious corporations. ICT supported democratic power will allow to reconsider the manifest of the other two forms of power: the elitist form and the sacred form.

Keywords: democracy, participative democracy, ICT, forms of power, structured information, personal assistant linker.

1. INTRODUCTION

"Freedom is the sure possession of those alone who have the courage to defend it."

Pericles

This paper outlines a CPSo project, called **iDemocracy** (**I**CT & **Democracy**), motivated by the following obvious observations:

- *the sustainable development of our way of life starts from a sustainable exercise of democracy all over the emergent global world;*
- *our world is confronted with the decline of how democracy works, because:*
  - the democratic mechanisms do not benefit from the tremendous technological development of the last two centuries (the "democratic technologies" are almost the same as the mechanisms used in the 18th century);
  - the democratic mechanisms are deeply affected negatively by some aspects of the technological development (at the beginning of the 3rd millennium the best communication technologies are used almost exclusively in a lot of non- democratic, maybe even anti-democratic activities, such as the process of brain washing designed and financed by big corporations).

This regress generates, under these circumstances, the following consequences:

- the emergence of corrupt political classes in countries that claim to be democracies;
- the emergence of alienated populations, resigned to live in corrupt democracies.

Project goal: reconsidering the way the democracy is exercised, from the perspective of the current and emergent information & communication technologies (ICTs), in order to balance the very critical relation established between the three entities which define our world: state, corporations and civil society.

2. CURRENT STATUS

The main technological achievements made in the last few decades in ICT

- are very efficiently fructified by the corporate space to corrupt the political class and to "sell" counterfeit images into the public space;
- are only partially assimilated by states helping them in solving only some simple administrative tasks;
- affect very little the civil society obsessively dominated by too "local" issues.

Immediate consequence: in our contemporary world the corporations gain preeminence in front of the state in the detriment of the civil society. Thus, all over the world the state "works" mainly for corporations and irresponsibly ignores the public interest.

Midterm consequence: the process of globalization takes place only at the level of the corporations, the states remain atomic entities, unable to act and interact globally, while the civil society's organizations become an amorphous space where unconstructive frustrations are accumulated.

The decline of democracy is due to the excessive control the corporate space has on how the democracy is exercised. To be clear, the proposed project does not question the concept of democracy, only the way democracy is exercised is reconsidered. Simply stated, how the technology can be

involved in balancing the potential material prosperity with an actual welfare.

3. PROJECT'S OBJECTIVES

The ***iDemocracy*** project has three, apparently very distinct, objectives:

- ***Defining new mechanisms of exercising democracy*** in the context of the new & emergent ICTs. The three powers of the state (legislative, administrative, judiciary) are kept separate, but their way to act must be deeply reconsidered, starting with the way the legislative power acts. The idea of a political class, fighting to get as many seats as possible in parliament where the laws governing the society are decided, is obsolete in the current circumstances dominated by the aggressive "lobby" financed by the corporate space;
- ***Defining the architecture of the information system*** designed to support the new mechanisms of exercising democracy. It will provide a two-direction flow of *structured information* (rather than the unstructured information which flows now inside the global information networks):
    a. from our complex world to each individual;
    b. from each individual towards the decision process using two ways:
        i. the *explicit* one, emulating ***a sort of participative democracy***, where each opinion/vote is weighted according to the tested competences of the participants (each voter, for each issue debated answers a set of specific questions in order to weight its vote);
        ii. the *implicit* one, allowed by a controlled openness each democratic player provides using a sort of "blog-based" continuous activity

  in order to make the use of ICTs directly helpful for individuals, to express their opinions and will, not only for corporations and/or specific governmental organizations.
- ***Developing the technological environment*** for the new architecture as a hierarchically interconnected network of
    - personal devices called **iPAL** (**I**CT **P**ersonal **A**ssistant **L**inker) used as an artificial ***pal*** which provides for its direct user the most appropriate and specific interface with our complex, savage and unpredictable world;
    - nodes equipped with low-power and high performance super computers working as intelligent data centers able to provide the preprocessed data used at the level of each iPAL

  as a system of direct use for the civil society and each human being in their interaction with the too greedy corporate network and with the too weak unstructured conglomerate of states.

Democracy, in danger in various forms all over the world, has no other chance to recover than by the action of the civil society projects, because the states and the political organizations are already under too much, more or less openly exercised, corporate control. With one condition: the civil society organizations must remain able to maintain their autonomy of thought and action. So, please pay attention to the sources and conditions of funding!

4. TECHNOLOGICAL ASPECTS

The specific technical aspects involved in the iDemocracy project must focus on two architectural levels:

1. iPAL architecture;
2. low-power supercomputer architecture for data center applications.

The current technology struggles to use, for these new specific functions, out of date architectural approaches developed in the last half of century for general purpose computation. This old approach was initially triggered by scientific and economic applications. The current market is driven by new and specific functional requests which require a fundamental rethinking of the architectural environment.

Computation is now one of the main existential resources of our society with two main poles: the individual and the global world. The individual uses various forms of iPALs, while at the global level a network of data centers provides the high level environment. We claim that both, the iPAL device and the data supercomputer must share the same kind of architecture: a cellular array of processing elements governed by a global loop, tightly interleaved with another cellular array of memories.

4.1 iPAL Architecture

A typical personal device, a sort of proto-iPAL, is the smart phone. The version recently proposed by ARM is represented in Fig.1. The heterogeneous computational resources are obvious. They are used to implement complex functionality, besides the calling function, such as:

- full Internet, including social networking;
- multimedia including HD video, and accessing full online content;
- GPS navigation and location;
- gaming using the latest OpenGL technology;
- messaging from SMS to e-mail.

We can identify in this architecture two kinds of processing elements:

- general purpose programmable resources, like various ARM cores, some of them equipped with NEON accelerators;
- specific programmable/configurable resources, like GPU and Video CODEC.

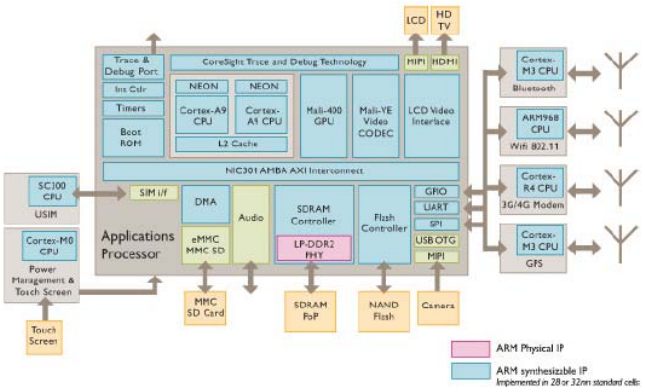

Fig. 1. ARM's smartphone architecture [ARM, (2012)]

These two types of resources were developed in the last decades as the ubiquitous pair processor–accelerator. The main limitation of this approach is given by the lack of an appropriate segregation between what we consider as being complex computation and intense computation. Both, complex and intense computation are supported by the same kind of architecture. The accelerator is based, correctly, on a parallel architecture, but the components of the resulting parallel engine are completely inappropriate.
The distinction between the complex computation and the intense computation is explained in (Ştefan (2009)) where:

- **complex** computation is characterized by the following main features:
  - mono or multi (few, no more than 8) big & **complex** processor organizations;
  - multi-threading programming model;
  - operating system oriented design;
  - cache-based memory hierarchy.
- **intense** computation is characterized by the following main features:
  - many (hundreds to thousands) **small & simple** cell organization;
  - vector and/or stream computing programming model;
  - high-latency functional pipe oriented system;
  - multi-buffer oriented memory hierarchy.

The difference between the two kinds of engines is quantified using two parameters:

- GOPS/Watt: Giga Operations per Second/Watt for energy efficiency ;
- GOPS/mm2: Giga Operations per Second/mm2 for area efficiency.

In (Ştefan (2009)) are used two architectures to illustrate the difference. For the complex computing an Intel implemented in 65nm, and for the intense computing the BrightScale's BA1024 implemented in 65nm are used. The results of the comparison are:

- (intGOPS/Watt)/(compGOPS/Watt) ~ 100
- (intGOPS/mm2)/(compGOPS/mm2) ~ 50

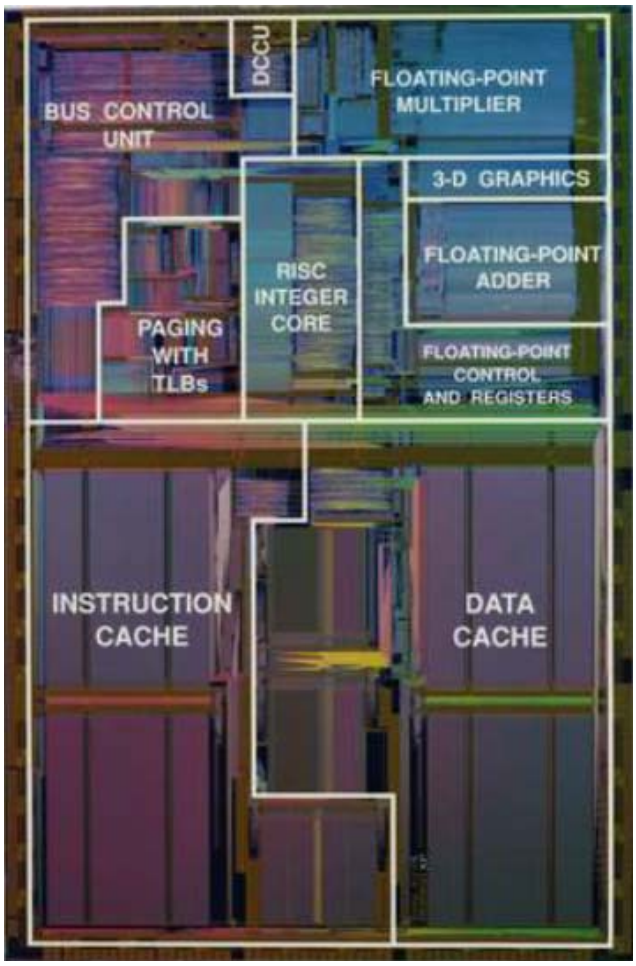

Fig. 2 i860TM XP Processor

How can we explain this big difference? By the way the physical resources are used in the current architectures designed for complex computation. In Fig. 2 is reproduced the layout of a typical complex processor in order to make only a rough estimation. The use of the area is edifying, because 56% is used for the cache memory, and the computing core is used more than 75% for floating point arithmetic.

If a processor designed for complex computing is used for intense computing, then the cache memory makes no sense, because both, program and data are accessed in a very predictable way, so 56% of the area is very inefficiently used. Then, while the float area is more than 75% from all the computational area, only the most intense floating-point oriented applications use around 24% floating-point operations [Hennessy & Patterson (2012)]. But, the average use of float operations is less than 10% percent. It follows that more than 90% of time more than 75% of the computational area is not used.

More, the area called RISC INTEGER CORE in Fig. 2 is designed with an execution pipeline of around 20 levels and the associated additional mechanisms (such as branch

prediction unit). The overhead introduced by this approach increases the area with non-computational features. If the bus control and MMU circuits are considered, then the computational active area on the chip is much less than 5% from the total area. The complex aspects of computation require a lot of extra-computational features which are completely useless for intense computation. Then, if a complex processor based engine is used for intense computation, then the level of inefficiency reaches unacceptable levels.

Now, let us see how is currently solved the problem of accelerators used for intense computations. The typical example is the NVIDIA architecture. One implementation is presented in Fig. 3.

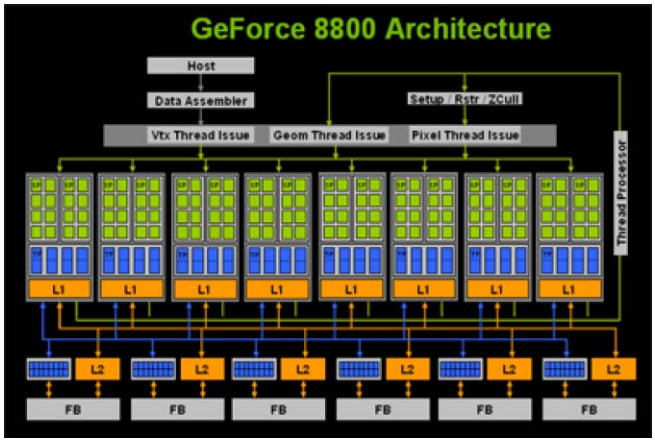

Fig. 3 GeForce 8800 GTX Block Diagram [NVIDIA, (2006)].

We will emphasize here only one incongruity. It is about the inexplicable occurrence of the two levels of caches in a system which runs the most predictable programs on the most predictable stream of data. Not to mention the complex organization of the computational cells in a two levels hierarchy with the subsequent complex programming environment.

The problem of intense computation cannot be solved replicating a complex engine in a complex organization. To make the story short, we mention only the huge power consumption of these architectures (hundred of Watts) and the big silicon area involved (sometimes exceeding 400 mm2). Designing an accelerator by multiplying complex computational resources is an ad hoc, completely wrong solution. In (Asanovic (2006)) the authors tell us that "small is beautiful" when it comes about the element used in designing a parallel computer. Let us try to follow this way! The architectural approach of the pair processor-accelerator must consider specific solutions for the two parts.

We define the architecture for an efficient parallel accelerator starting from Backus's concept of Functional Programming System (FPS) (Backus (1978)) and Sabot's Paralation Model (PM) (Sabot (1988)). A parallel accelerator must support all functional forms proposed by Backus in its seminal paper. They are also compatible with Sabot's model applied to the one-chip parallel engine. The main functions and functional forms used to define the architecture of a parallel accelerator are:

- **Apply to all** : represents data-parallel computation of form:
  $$\alpha f<x1,\ldots, xp> \rightarrow <f:x1,\ldots, f:xp>$$
- **Insert** : represents reduction-parallel computation of form:
  $$/f:<x1,\ldots, xp> \rightarrow f:<x1,/f:<x2,\ldots, xp>>$$
- **Construction** : represents speculative-parallel computation of form:
  $$|f1,\ldots, fp|:x \rightarrow <f1:x,\ldots, fp:x>$$
- **Composition** : represents time-parallel computation of form:
  $$(fq \circ fq\text{-}1 \circ \ldots \circ f1)|:x \rightarrow fq:(fq\text{-}1:(fq\text{-}2:(\ldots:(f1:x)\ldots)))$$
- **Threaded construction**: represents the thread-parallel computation, a special case of construction for $fi = gi \circ i$, of form:
  $$\theta(f1,\ldots, fp):<x1,\ldots, xp> \rightarrow <g1:x1, \ldots, gp:xp>$$
- **Permute** : defined on two equally length sequences, one defining the permutation, while the second is submitted to permutation, as follows:
  $$perm:<<y1\ldots, yp>,<x1,\ldots, xp>> \rightarrow <xy1,\ldots, xyp>$$
- **Selector** : returns the i-th element of a sequence, as follows:
  $$i: <x1,\ldots, xp> \rightarrow xi$$

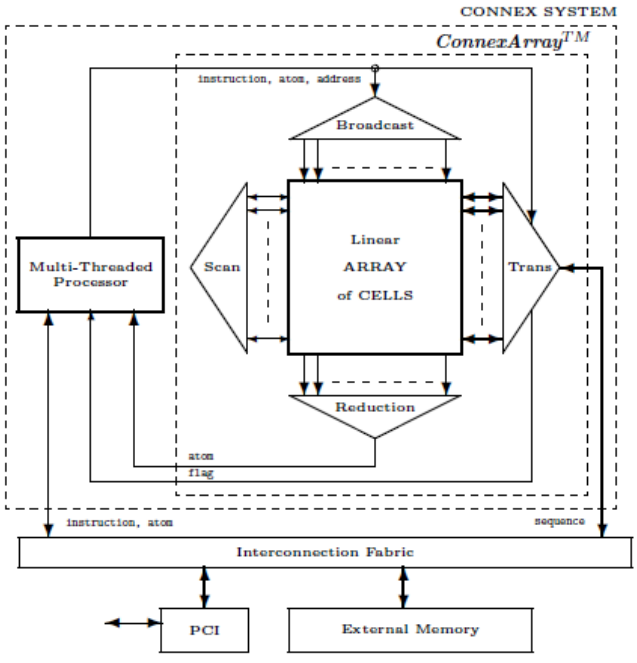

Fig. 4 The Connex System

We called such an architecture Integral Parallel Architecture (IPA) (Maliţa & Ştefan (2009)). ConnexArrayTM is the first partial embodiment of an IPA. It is already implemented in few versions for video applications (Ştefan (2006)).

The block schematic of the Connex System containing ConnexArrayTM is represented in Fig. 4, where:

- **Linear Array of Cells** : contains small & simple processing elements or execution units;

- **Multi-Threaded Processor** : issues in each cycle the instruction to be executed at the level of each cell according to the internal state of each cell;
- **Broadcast** : is a log-depth distribution network for the instruction issued by the Multi-Threaded Processor;
- **Reduction** : is a log-depth reduction network (for add, max, select);
- **Scan** : is a log-depth global loop closed over the array of cells;
- **Trans** : is the transfer system which loads or stores vectors of data from/to memory.

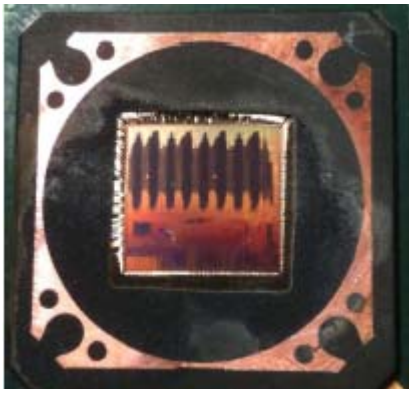

Fig. 5 The Connex Chip.

The last version of the Connex System was implemented in 2008 as part of BA1024 chip, a 1024-cell array of 16-bit cells, each having 1KB of local data memory. The 65 nm technology with a standard cell design provided 400 GOPS performance with: >120 GOPS/Watt and >6 GOPS/mm2.

Going back to the Fig. 1, the architecture of a smart phone can be substantially improved using for the computational part a Connex System, where for the complex part of the computation is in charge the Multi-Threaded Processor, while for the intense part of computation a ConnexArrayTM with no more than few hundred cells is associated. Thus, the way toward a real iPAL is opened.

4.2 Data Supercomputer Architecture

The second architectural level involved in the iDemocracy project is the low-power supercomputer architecture for data center applications. The overall aspect of computation involved at this level is almost exclusively intense. The cellular approach is mandatory for reasons similar with those used at the iPAL level. For this reason a recursive definition for the organization of the low-power supercomputer is possible. In Fig. 6 the cellular frame is defined. It describes an organization with two fine-grain interleaved networks: one of computation engines and another of memories. The controller is a sequential engine and the memory buffer is part of the buffer-based memory hierarchy. This cellular architecture applies also for the definition of Engine modules it contains. Each Engine has, recursively, the same organization. The only difference is quantitative. While at the first level of the supercomputer Memory block represents a HDD/SSD 4-16 TB, at the level of each Engine, Memory is a SRAM of 4-16 KB.

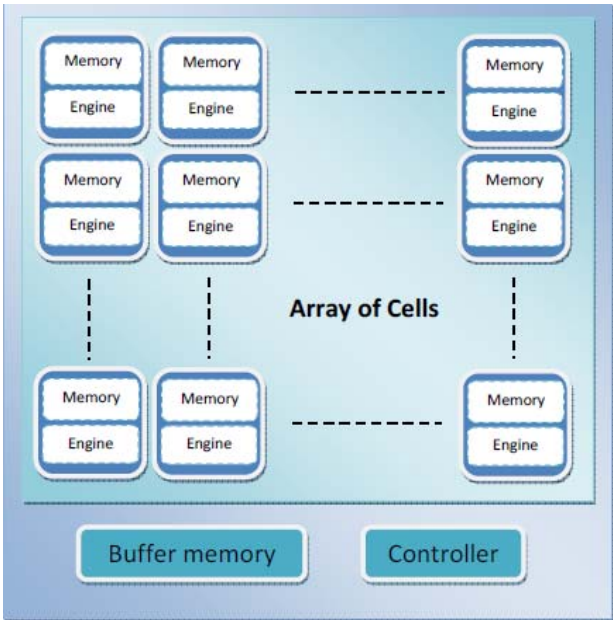

Fig. 6 The recursive cellular architecture applied to define the low-power supercomputer organization.

The number of cells considered on each level could be similar. Around 1024 cells is a reasonable size for the next decade. A peta-byte machine is estimated as a supercomputer system consuming around 15 KWatt with around 1 million elementary processing elements.

5. MODE OF ACTION

While the technical implementation must be fast and aggressive, the use of technology in the iDemocracy project must be considered a gradual process, with many iterative stages, because of the big "time constants" associated to any evolution inside our complex society. We must avoid stressing too much our very reluctant world! Because all the three main components of our world – civil society, corporations, states – are characterized by highly inertial processes, any new mechanism of exercising democracy must be initially implemented as an alternative and experimental process working in parallel with the currently used parliamentary mechanisms.

The main effect of the gradual implementation of iDemocracy will be the transition toward the integral way of exercising power in our world, which implies the following three forms:

- the **democratic** form of power, as a ***rational*** exercise of the threefold competences of the state: the legislative, the administrative and the judiciary
- the **elitist** form of power, as the action of the ***imaginative*** power of a body of highly competent people, able to provide solutions validated democratically under the sacred power supervision

- the **sacred** form of power, as an unquestionable ***spiritual*** power, which offers the superior discernment when *reason* is too harsh or *imagination* is too heated.

The current use of democracy implies only theoretically the imaginative and the spiritual attitudes, but it is unable to provide effective mechanisms for involving them in the actual exercise of power. The quasi general inefficiency and corruption of the political/administrative/judiciary class all over the world is generated by the lack of imagination in the solutions they propose and the unethical readiness to accept solutions imposed by the persuasive financial power of corporations.

If ***Democracy → iDemocracy***, then a lot of technical and formal aspects will be performed by incorruptible engines, democracy will tend to be participative, *avoiding* ***gradually*** *the corrupt representatives*, and, under the supervision of the untouchable sacred power, ***apolitical*** elites will take care of proposing solutions for the problems of our too fast changing world.

Few comments about the words *"sacred"* and *"spiritual"* must be added. The two terms have the meaning established by a long and inappropriate use for limited religious purposes. In fact, the two terms are deeply related with the holistic connection of each human being with existence as a whole. The genuine sacred or spiritual attitude is beyond any form or structure, and ignores any religious, cultural or customary delimitation. Unfortunately, the two terms are currently used to designate almost exclusively religious and/or mystical attitudes. Maybe in time the religious and mystical connotations will fade away and the original meanings, related to the wholeness, will prevail. In this respect Mircea Eliade states very clearly:

"It is unfortunate that we do not have at our disposal a more precise word than "religion" to denote the experience of the sacred. ... But perhaps it is too late to search for another word, and "religion" may still be a useful term provided we keep in mind that it does not necessarily imply belief in God, gods, or ghosts, but refers to the experience of the sacred, and, consequently, is related to the ideas of being, meaning*, and* truth*."*

[Eliade (1969)]

Maybe it is time to start the process of reconsidering the meaning of terms such as *spiritual* or *sacred,* freeing them from limited and distorted religious or mystic connotations. We hope it is not "too late to search" for all the real meanings which lay behind a term such as *sacred*. Restoring the secular meanings associated with *spiritual* and *sacred* will allow the use of these terms in creating a new existential perception.

The *arbiter* must be sacred and the proposals must emerge from *elites*, while the *decision / implementation / trial* must be done democratically. Thus, ***sacred – elitist – democratic*** is the **power triad** (see Ştefan (2010)) able to balance our too disturbed world. This triad corresponds with the triad associated to the deep human mind behaviour:

spirituality – imaginary – reason

Maybe it is normal that the way power is exercised to correspond to the threefold behaviour of the human mind.

In an advanced stage of the process, *artificial forms of consciousness* (see Drăgănescu, M. (2007)) will act in all forms of power. If it will be possible, then our troubled world will reach a temporary state of equilibrium (obviously only till new forms of human fraudulent behaviours will emerge). We are obliged to consider in the near future new ICTs able to support, sometimes substitute, even the natural and historical forms of the sacred power. CPSo technologies have the chance to be very supportive only for the two extremes, maybe less human, components of the power triad: the rationally controlled *democratic* power and the spiritually exercised *sacred* power. It will be less supportive for the *elitist* form of power, because this form is related to the most human and natural form of mental behaviour, the imaginary with its three forms: will, intuition, fantasy. The closeness between reason and spirituality is surprisingly well emphasized by Lev Tolstoi in his diary entry from 28th of May 1907 where he wrote:

"There are two sciences: mathematics and ethics. One is the superficial, the other is the deepest. These sciences are accurate and unambiguous because all people have the same reason which receives mathematics and the same spiritual nature which receives moral."

[Tolstoi (2009)]

There are a lot of reasons to consider that both the democratic power and the sacred power are able to receive a consistent technological ICT support. More than that, there is the chance that the sacred power is to be exercised only by advanced artefacts able to consider the huge complexity of the existence, which includes our world and our unpredictable humanity.

6. CONCLUSIONS

The rational form of power – the democratic power - cannot survive without an explicit support received from ICTs. The *iDemocracy* project will provide the coherent framework where democracy and technology meet. Democracy, fertilized with the last ICTs, will give rise to the *integral way of exercising power* which provides a good balance between the three forms of power: democratic, elitist and sacred. *Artificial forms of consciousness* will support all forms of power, mainly the democratic and the sacred. ICTs are in the position to improve our rational and spiritual behavior freeing the imaginative behavior from the oppressive limitations imposed by our weak reason and lost sacredness.

7. ACKNOWLEDGMENTS

The author got a lot of support from the main technical contributors to the development of the ConnexArrayTM technology, the BA1024 chip, the associated language, and its first application: Emanuele Altieri, Frank Ho, Mihaela Maliţa, Bogdan Mîţu, Marius Stoian, Dominique Thiebaut, Tom Thomson, Dan Tomescu.

REFERENCES

ARM (2012), *The Architecture for the Digital World*, at http://www.arm.com/markets/mobile/smartphones.php

Asanovic, Krste, et. al. (2006). "The Landscape of Parallel Computing Research: A View from Berkeley", *Technical Report No.UCB/EECS-2006-183*. http://www.eecs.berkeley.edu/Pubs/TechRpts/2006/EECS-2006-183.pdf

Backus, John. (1978). "Can programming be liberated from the von Neumann style? A functional style and its algebra of programs", *Communications of the ACM*, 21, 8 (August).

Drăgănescu, Mihai. (2007). *Societatea conştiinţei (The Society of Consciousness), ICIA, Bucharest.* (in Romanian)

Eliade, Mircea. (1969). *The Quest. History and Meaning in Religion*, The University of Chicago Press.

Hennessy, John L., David A. Patterson (2012). *Computer Architecture. A Quantitative Approach*, Fifth Edition, Morgan Kaufmann.

Maliţa, Mihaela, Gheorghe M. Ştefan (2009). "Integral Parallel Architecture & Berkeley's Motifs", *ASAP09 - 20th IEEE International Conference on Application-Specific Systems, Architectures and Processors*, 7-9 July, 2009, Boston, MA.

McCool, Michael D. (2008). "Scalable Programming Moeles for Massively Multycore Processors", *Proceedings of the IEEE*, Vol. 96, No. 5, May 2008.

NVIDIA (2006), *NVIDIA GeForce 8800 GPU. Architecture Overview*.

Sabot, Gary W. (1988). *The Paralation Model. Architecture-Independent Parallel Programming*, The MIT Press.

Ştefan, Gheorghe M., et al. (2006). "The CA1024: A Fully Programmable System-On-Chip for Cost-Effective HDTV Media Processing", *Hot Chips: A Symposium on High Performance Chips*, Stanford Univ., August, 2006.

Ştefan, Gheorghe M. (2009). "One-chip TeraArchitecture", *Proceedings of the 8th Applications and Principles of Information Science Conference*, Okinawa, Japan on 11-12 January 2009.

Ştefan, Gheorghe M. (2010). *Ethos – Pathos – Logos*, All Pub. House, Bucharest. (in Romanian)

Tolstoi, Lev Nikolaevici. (2009). *Despre Dumnezeu şi om. Din jurnalul ultimilor ani (About God and Men. From the Last Years Diary)*, Humanitas, Bucharest. (in Romanian)